Wafer Sub-Layer Impact In OPC/ORC Models For 2x nm Node Implant Layers

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ABSTRACT

From 28nm technology node and below, Optical Proximity Correction (OPC) needs to take into account light scattering effects from prior layers when bottom anti-reflective coating (BARC) is not used, which is typical for implant layers. In this paper, we implement a sub-layer aware simulation method into a verification tool for Optical Rule Check (ORC) that is used on full 28nm test chip. The sub-layer aware verification can predict defects that are missed by standard ORC. SEM-CD review and defectivity analysis were used to confirm the validity of the sub-layer aware model on wafer.

Keywords: OPC, stack effect, wafer topography, model, lithography, mask, implant

1. INTRODUCTION

With advanced technology nodes, the CD and overlay control of implant layers are becoming critical. As the distances designed between implant boundaries and active regions decrease, the CD error tolerance of implant patterning cannot remain as loose as before. Some implant layers are patterned using a Developable Bottom Anti-Reflective Coating (DBARC) but, for cost and technical concerns, most of the implant layers do not benefit from BARC. In this last case, implant patterning is significantly impacted by the reflections from the sub layers present on the wafer. The patterning of pre-gate implant layers is affected by active silicon and silicon oxide Shallow Trench Isolation (STI) patterns. For post-gate implant layers, both active patterns and poly silicon patterns contribute to undesirable reflections. An example is represented on figure 1.

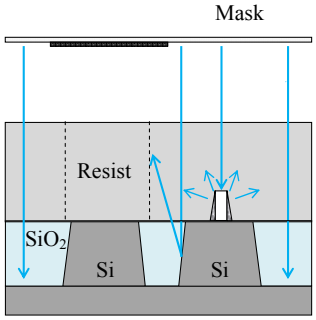

Figure 1. Schematic of resist patterning of post-gate implants. The arrows represent the light reflection and scattering effects due to the sub layers.

In a previous paper [1], we have proposed a simple method to empirically model the sub layer effects on lithography. It is based on a fictive mask approach. After a brief description of this fictive-mask concept, we will present how we have implemented this method in our ORC flow and run a full-chip sub-layer aware verification for source-drain implant patterning. We will discuss the results and give our perspectives.

2. FICTIVE-MASK METHOD FOR SUB-LAYER AWARE SIMULATIONS

2.1 Fictive-mask concept

The ability of modeling the sub-layer effects on lithography is a necessity for OPC/ORC of 2x-nm node implants, however, for runtime considerations, we cannot adopt a rigorous model that fully solves the electro-magnetic equations. We are exploring the possibility of using an empirical model directly based on the observation of SEM-CD measurement

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results. We empirically quantify the effect of the sub layers on the wafer CD of the main layer, i.e. of the implant layer. And, like new commercial OPC/ORC solutions [2-3], we add components, into the conventional simulation tool, that aim to reproduce the sub-layer effect on the simulated implant CD. Our in-house method consists in transposing the effects that actually happen in the near field of the wafer onto the mask, in the object plane of the optical lithography system. This method can be easily implemented into the existing OPC/ORC commercial platforms, and in the same time, it affords a lot of flexibility.

Figure 2 is a schematic of our concept. The model used (optical model and resist model) is conventional. We calibrate it with implant patterns on bare silicon. It is the mask transmission that we modify so as to simulate the sub-layer effects. We call fictive mask the mask resulting from this modification. It is composed of the main implant layer plus some derived layers that we generate with Boolean operations (during the ruled-based OPC run for instance).

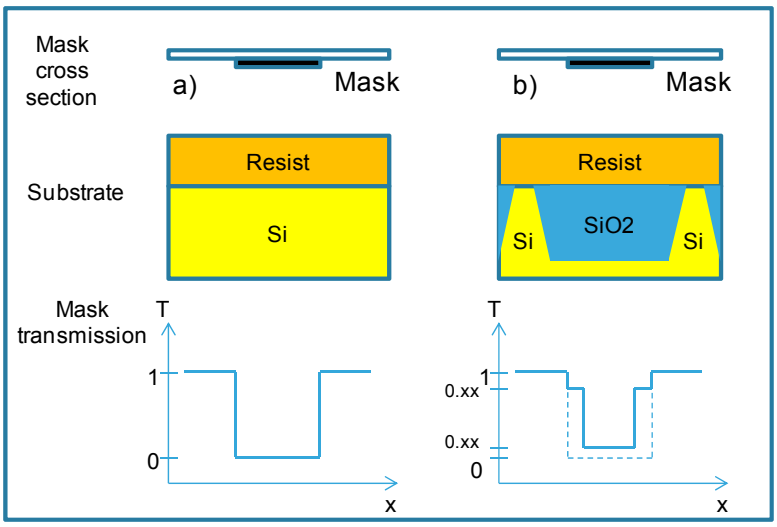

Figure 2. Example of simulation of an isolated resist line. On a bare silicon wafer (a), the mask transmission is unchanged. When active/STI patterns are present (b), the fictive mask takes into account the sub-layer effects.

Six derived layers are used. They address three effects:

- the effect of the STI stack, compared with the Si stack of the model,
- the effect of the Si/STI transitions,
- the effect of the poly structures.

Our calibration consists in adjusting the shape parameters and the transmission coefficients of the derived layers in order to match the CD differences observed on wafer. With the polygon shapes, we manage the distance range of the sub-layer effects. With the transmission coefficients, we can tune the strength of each sub-layer effect.

Note that the rules to manage the polygon shapes have changed in this paper compared with our last work [1]. We present improved calibration results.

2.2 Calibration

Our starting point is a model calibrated with implant structures measured on bare silicon (~100 structures). In addition of that, in order to calibrate our sub-layer aware simulation flow, we have measured implant structures patterned on a wafer with sub layers (~400 structures). Three families of implant structures are used for calibration: structures on a large STI region, structures on an active sub layer (active patterns), and structures on a poly sub layer (poly patterns).

Our set of structures includes various geometries: lines and spaces, 1D (one-dimension) and 2D (2-dimension) structures, isolated and dense structures. The sub-layer effect, expressed in nanometers, is the difference between a CD measured on a sub layer and the CD of reference, measured on bare silicon. The calibration consists in fitting the measured sub-layer effect with our simulations for all the structures.

At the end of the calibration, the geometrical parameters of the rules to build the layers and the transmission of the six layers that compose the fictive mask are determined. See the results of our sub-layer aware simulation flow on figure 3.

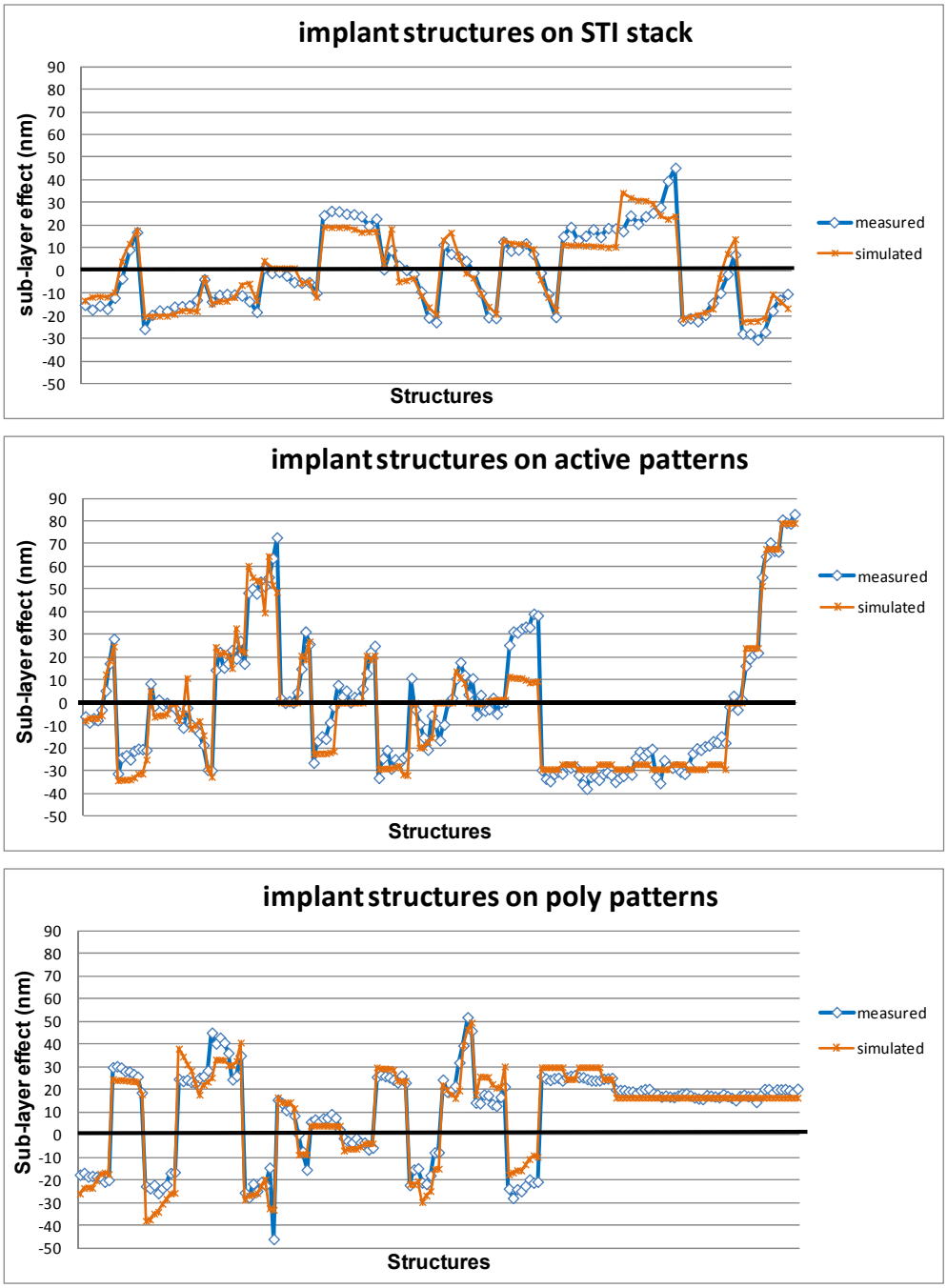

Figure 3. Sub-layer effect: measured data and simulated data for three families of structures. The sub-layer effect is defined as the difference between the CD measured on the sub layer and the CD measured on bare silicon.

These data, expressed in nanometers, can be directly related to the CD control requirements. It is interesting to compare the strengths of the different sub layer effects. We find the strongest effects among the structures on active patterns: up to 80nm. Our simulations re-produce the sub-layer effects very well.

The model error, expressed as a percentage of the wafer CD, is also an important result to report. We have not plotted this result on a figure here but the global result is very satisfying too. Among the above structures, the conventional model shows errors as large as 50%. Our sub-layer aware simulation is much more accurate: the error is below 12% for all the structures.

3. FULL-CHIP SUB-LAYER AWARE VERIFICATION

The fictive-mask concept can be either implemented for OPC or for ORC (see the possible flows in reference [1]). Our need for the 28nm technology node is to perform reliable full-chip verification before mask ordering. We have used the "fictive-mask" method for Optical Rule Check. We have run a standard OPC and then, a sub-layer aware ORC. In this work, we have built the fictive mask after the OPC flow:

- We have run our rule-based script to generate the fictive layers.
- We have run the ORC simulations through this fictive mask composed of layers of different transmissions.

3.1 ORC results

ORC consists in simulating the resist contours on the whole chip after the OPC run and identifying the lithography hotspots by means of width and space checks. We have run ORC for implant patterning at source-drain level (both active and gate structures are present on the substrate). Here are the results of our ORC run, with and without sub-layer aware simulations:

	Conventional model	Sub-layer aware simulation
Total number of defects	2 776	135 000
Worst resist necking value	157 nm	98 nm
Worst resist bridging value	147 nm	104 nm

The CDs of the resist lines and trenches, out of the conventional OPC, appear to be more critical when we do not ignore the sub-layer effects. Using the same defect threshold values, the sub-layer aware simulations predict much more necking and bridging risks than the conventional model.

Note that the runtime penalty of the sub-layer aware simulation is 30%. Since the ORC represents about 20% of the overall mask data preparation (OPC + ORC), this 30% increase in ORC adds less than 10% to the total runtime.

3.2 SEM images through process window

Among the ORC defects found using our sub-layer aware simulation flow, we have chosen about twenty defects to inspect them through process window with SEM-CD measurements. As an example, Figure 4 illustrates the distribution of the resist necking defects. We have plotted circles that show the ORC defects, chosen in this defect population, to be reviewed with SEM-CD.

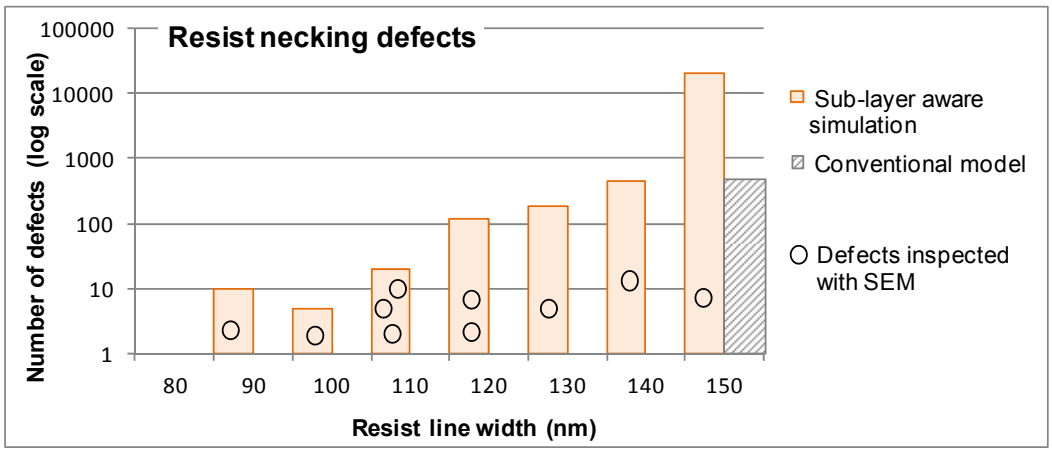

Figure 4. Distribution of the resist necking defects: sub-layer aware ORC compared with conventional ORC.

SEM-CD measurements reveal that half of the selected ORC defects are true alerts: we observe that these structures have substantially smaller process window compared to the specification defined for production.

Figures 5 and 6 are examples of these defects. Both of them are resist necking hotspots. On the layout view, we have represented the simulation through the conventional model and the simulation contour using our sub-layer aware flow. Only the ORC run with the sub-layer aware simulation alerts us on these hotspots.

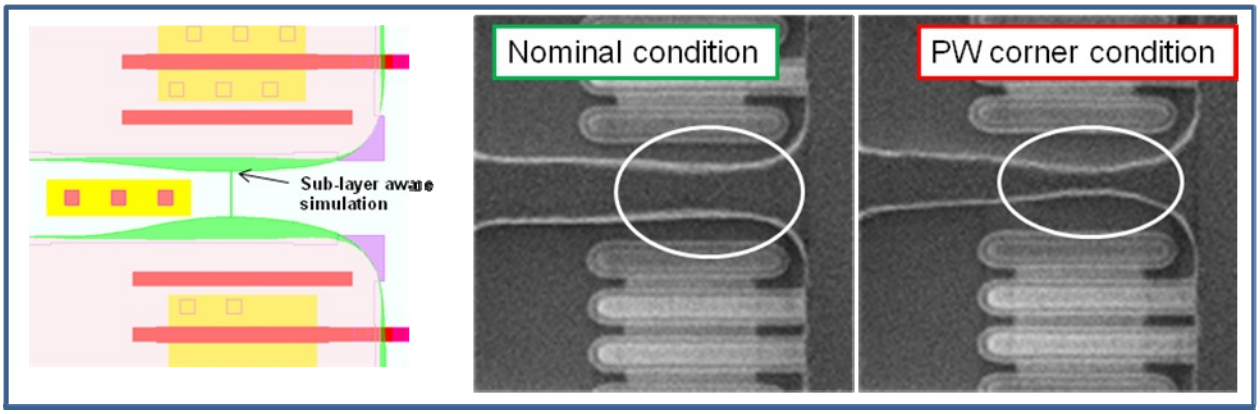

Figure 5. Layout view of an ORC defect with sub-layer aware simulation of the implant patterning at nominal condition. SEM images of this implant structure after lithography on a Focus Exposure Matrix.

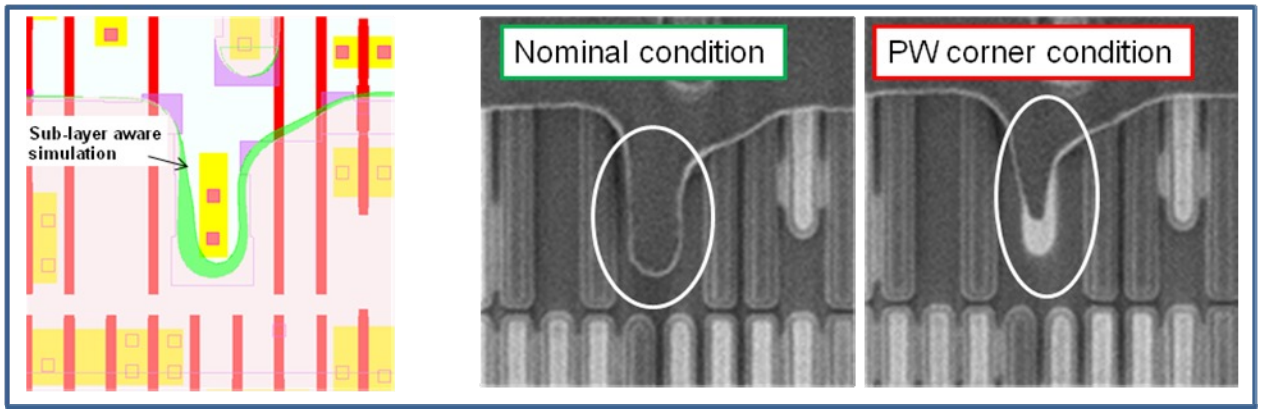

Figure 6. Layout view of a second ORC defect with sub-layer aware simulation of the implant patterning at nominal condition. SEM images of this implant structure after lithography on a Focus Exposure Matrix.

3.3 Defect inspection

Another test chip has been inspected with an optical defect inspection tool using Process Window Qualification (PWQ) methodology [4]. This verification step gives key information during the development of a technology. It is the wafer verification that we can rely on to find defects that we are not able to simulate yet.
The PWQ compares dies exposed with off-nominal lithography conditions to dies exposed at the nominal process condition. It identifies the repeating defects within a given process window. This inspection is independent of the OPC model, thus it is very useful for OPC model verification in a cross check mode.

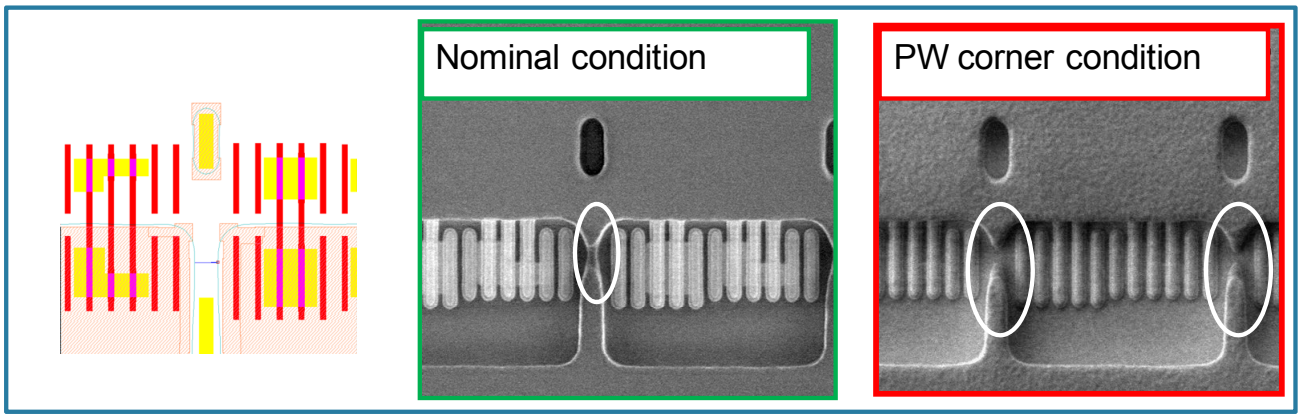

Figure 7. Hard necking defect caught with the optical defect inspection tool.

The defect inspection tool has caught one defect within the process window of our implant layer. It is shown in Figure 7: it is resist necking and the resist line even opens at the corner of the Process Window. This defect belongs to the necking hotspots identified with sub-layer aware ORC run. Even though the simulated CD does not exactly match the wafer data the necking trend is correctly predicted with the sub-layer aware simulation. This is a major step towards efficient OPC verification.

4. DISCUSSION

We have used two techniques to check the reliability of our sub-layer aware simulations: SEM-CD review of the ORC hotspots and PWQ methodology on a full test chip. Though not all the sub-layer aware ORC defects are true alerts, we were able to demonstrate a clear improvement in terms of predictability of patterning issues over conventional models. Further improvements are expected by better taking into account the combined effects of active patterns and poly patterns. This implies to further adjust our rules and to use even more calibration patterns.

Sub-layer aware ORC gives us the ability to take corrective actions before ordering the implant mask. In this study, we have identified a lot of critical patterns. Fortunately, most of these defects do not concern functional parts of the design, they have no electrical impact. A first action, after these observations, has been to better clean the design layout to prevent nonfunctional, but contaminating, defects like pattern collapses. As a containment, the CD and overlay specifications have been tightened to mitigate the observed patterning risks. Finally, for yield-critical defects we implement rule-based corrections on the target of specific patterns.

If the sub-layer effects are too serious, they cannot be ignored during OPC. We also consider implementing a full sub-layer aware OPC/ORC flow.

5. CONCLUSION

It is a necessity today, for OPC on implant layers without BARC, to develop a tool for full-chip sub-layer aware verification. In this paper, we have proposed an in-house solution. The “fictive-mask” method shows good results on a large set of calibration patterns. Moreover, it is compatible with EDA tools to run full-chip verification. The developed sub-layer aware verification has been run on a 28nm test chip with acceptable runtime penalty. The defects resulting from this verification have been compared to SEM images through process window and to the defects caught at the defectivity inspection step. The solution needs to be improved to better match wafer results. However, there is a clear gain over conventional verification. Our check has highlighted a lot of critical defects (missed by the conventional ORC), among which the hard-necking defect caught with defectivity inspection. This is very important for us not to ignore the sub-layer effects anymore and to anticipate the hotspots before we order the mask. Our perspective is to improve the “fictive-mask” method in order to better take into account the combined effects of active and poly patterns.

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